Docket No.: 30205/39380

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES LETTERS PATENT

Title:

CMP SLURRY COMPOSITIONS FOR OXIDE FILMS AND METHODS FOR FORMING METAL LINE CONTACT PLUGS USING THE SAME

Jong Goo JUNG

#145-1903 Hwanggol Jugong Apt., 955-1
Yeongtong-dong, Paldal-gu, Suwon-si,
Gyeonggi-do 442-470
Korea

Sang Ick LEE

#704-1901 Hyundai 7-cha Apt., 753
Ami-ri, Bubal-eup, Icheon-si
Gyeonggi-do 467-860
Korea

CMP SLURRY COMPOSITIONS FOR OXIDE FILMS AND METHODS FOR FORMING METAL LINE CONTACT PLUGS USING THE SAME

BACKGROUND

Technical Field

A chemical mechanical polishing (CMP) slurry for oxide film and a methods for forming a metal line contact plug of a semiconductor device using the same are disclosed. More particularly, the disclosed methods for forming metal line contact plugs can form a stable landing plug poly (LPP) by performing a polishing process of a multi-layer film by using the CMP slurry for oxide film including an HXOn compound (wherein n is an integer from 1 to 4).

Description of the Related Art

In order to provide a small, large capacity and highly integrated semiconductor device, after forming a transistor, a bit line and a capacitor for the device, a subsequent process for forming a multi-layer line such as a metal line for electrically connecting the respective elements needs to be performed.

In general, when a subsequent conventional process for forming a metal line is performed, a planarization process must be performed by polishing multiple layers simultaneously by using a single slurry before a deposition process or etching process.

However, when multiple layers are polished by using a single slurry, each layer has a different polishing speed, namely a different polishing selectivity ratio to the slurry, and thus step differences are generated between the layers which is problematic.

Further, polishing residues of each layer and abrasive residues in the slurry tend to fill the upper portion of the interlayer insulating film because of the high step difference generated in the interlayer insulating film due to its higher polishing speed than the other layers. As a result, defects such as bridges between plugs of the device are generated.

The conventional process for the semiconductor device will be explained in detail with reference to the accompanying drawings.

Referring to Fig. 1A, a process for forming a LPP is observed in a section A-A' of a plan diagram showing a general word line pattern 4.

Referring to Fig. 1B, a conductive layer for word line (not shown) is deposited on a cell area of a semiconductor substrate, namely silicon substrate 1, a hard mask film (i.e., a

nitride film not shown) is deposited on the conductive layer for word line at a thickness of t1 (1500 to 3200 Å). Then, word line pattern 4 having a hard mask pattern 3 on a conductive layer pattern 2 for word line is formed by sequentially etching the hard mask film and the conductive layer for word line.

A spacer 5 is formed on the sides of the resulting structure, and an interlayer insulating film 7 is formed on the entire surface of the resulting structure at a thickness of t2 (5000 to 8000 Å). The interlayer insulating film 7 is planarized.

Referring to Fig. 1C, the thickness of the interlayer insulating film 7 decreases from t2 to t4 (4500 to 7500 Å) according to the planarization process (t2>t4).

An etching process for forming a contact hole 8 for plug by using a landing plug contact mask (not shown) is performed on a predetermined portion of the cell region. Here, since the upper portion of the hard mask pattern 3 is also etched, the thickness of the hard mask pattern decreases from the initial thickness t1 to t3 (1000 to 2500 Å) (t1>t3).

Referring to Fig. 1D, a region (a) where the contact hole 8 for plug is not formed and a region (b) where the interlayer insulating film is removed to form the contact hole 8 are formed according to the etching process. It is observed in section B-B' as shown in Fig. 1E.

Referring to Fig. 1E, a silicon layer 9 is deposited on the entire surface of the resulting structure including the contact hole 8 for plug. Here, the silicon layer 9 has step difference of t5 (1000 to 2000 Å) due to step difference between the regions (a) and (b).

Thereafter, a plug 11 is isolated by a succeeding polishing process. Preferably, a thickness to be removed is greater than t6 (2200 to 3200 Å).

Referring to Fig. 1F, a CMP process is performed on the entire surface of the silicon layer 9 and the interlayer insulating film 7 by using a general slurry for oxide film until the hard mask pattern 3 is exposed, thereby forming the plug 11.

The slurry for oxide film used in the above CMP process is a general CMP slurry for oxide film having pH of 2 to 12 and includes an abrasive such as colloidal or fumed SiO_2 or Al_2O_3.

In general, a slurry having a similar polishing speed among the multi-layers must be used to remove a multi-layer film. However, when the general single slurry for oxide film is used in the conventional CMP process, the polishing speed of the interlayer insulating film

has a higher polishing selectivity ratio than that of the word line hard mask film or silicon layer by at least three times.

Therefore, a step difference t7 of 400 to 500 Å (Fig. 1F) is generated between the hard mask nitride film pattern 3 and the silicon layer 9, and a step difference t8 of 460 to 700 Å is generated between the hard mask nitride film pattern 3 and the interlayer insulating film 7 after the polishing process due to differences of the polishing selectivity ratio.

Further, polishing residues of each layer and abrasive residues from the slurry fill in the upper portion of the interlayer insulating film 7 that has a relatively high step difference from the hard mask nitride film pattern 3.

Referring to Fig. 1G, the abrasive residues of the CMP process are filled in the upper portion of the interlayer insulating film 7, to generate "Pinocchio" defects 17. The "Pinocchio" defects 17 are generated during the process for isolating the plug 11 due to dishing of an oxide film having a high polishing selectivity ratio to the nitride film.

The step difference is observed in a section C-C' (Fig. 1H).

Referring to Fig. 1H, step differences are generated between the hard mask pattern 4 and the silicon layer 9, and between the hard mask pattern 4 and the interlayer insulating film 7 formed in the cell region of the substrate 1 due to differences of the polishing selectivity ratio after the polishing process using the CMP slurry for oxide film.

When the conventional single slurry is used in the CMP process for polishing the multiple layers, the step differences and Pinocchio defects are generated to form a bridge between plugs and increase leakage current. As a result, mis-alignment is generated in a succeeding process, and thus the manufacturing yield is reduced.

SUMMARY OF THE DISCLOSURE

A CMP slurry for oxide film having a similar polishing selectivity ratio to multiple layers is disclosed herein.

A method for forming a metal line contact plug of a semiconductor device which forms a stable plug by using the CMP slurry for oxide film is disclosed herein.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A through 1F are schematic diagrams illustrating a conventional method for manufacturing a semiconductor device using a CMP process.

The conventional Figs. 1G and 1H are photographs taken after a process for isolating a plug is carried out.

Figs. 2A through 2D are schematic diagrams illustrating a disclosed method for forming a metal line contact plug of a semiconductor device according to a disclosed CMP process using a slurry disclosed herein.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

A disclosed CMP slurry composition for oxide film comprises a solvent, an abrasive dispersed in the solvent and an HXOn compound (wherein n is an integer from 1 to 4).

The solvent of the slurry composition is distilled water or ultra pure water, and the abrasive includes colloidal or fumed silica (SiO_2) having a grain size of 20 to 300 nm, alumina (Al_2O_3) or ceria (CeO_2).

The silica is present in an amount of 15 to 25 wt%, the alumina is present in an amount of 5 to 15 wt% and the ceria is present in an amount of 5 to 15 wt% in the slurry.

The slurry has pH below 7, preferably ranges from 2 to 5.

X of the HXO_n compound is a halogen compound such as F, Cl, Br or I. Exemplary HXO_n compounds include HIO_4, HClO, $HClO_3$, $HClO_4$, $HBrO_3$ or HIO_3, preferably HIO_4.

The HXO_n compound is present in an amount ranging from 0.01 to 10 wt%, preferably from 0.1 to 5 wt% in the slurry.

In general, an oxide film and a silicon layer has a lower polishing selectivity ratio than the nitride film when the acid slurry is used.

Here, the HXO_n compound is used as a pH control agent for increasing the polishing selectivity ratio of the nitride film and decreasing the polishing selectivity ratio of the oxide film.

That is, the CMP slurry composition for oxide film of the present invention includes the HXO_n compound, and thus the polishing selectivity ratio of an interlayer insulating film

formed of an oxide film to a nitride hard mask film is 1:3, preferably 1:2, and the polishing selectivity ratio of the oxide film to the silicon layer is 1:3, preferably 1:2.

In addition, the HXO_n compound is used as an oxidant for increasing the polishing speed of the silicon layer by forming an oxide film which can be easily polished on the silicon surface.

The CMP slurry composition for oxide film of the present invention comprising the HXO_n compound allows the respective multiple layers to have a similar polishing selectivity ratio, so that the layers can be polished in a similar speed.

As a result, step differences are not generated between the layers after the CMP process, and thus polishing residues of each layer and slurry residues are not filled in the upper portion of the interlayer insulating film during the polishing process.

A disclosed method for forming a metal line contact plug of a semiconductor device comprises:

depositing a conductive material for word line on a semiconductor substrate;

forming a word line pattern by depositing a hard mask nitride film on the overlap portion of the conductive material for word line;

forming a nitride film spacer at the side of the word line pattern;

forming a planarized interlayer insulating film on the word line pattern;

forming a contact hole by etching the interlayer insulating film until the substrate is exposed;

forming a silicon layer on the surface of the interlayer insulating film having the contact hole; and

performing a CMP process on the silicon layer and the interlayer insulating film until the hard mask nitride film is exposed, by using a CMP slurry composition for oxide film including a solvent, an abrasive dispersed in the solvent and an HXOn compound.

Preferably, the interlayer insulating film is formed of an oxide film.

The disclosure methods will be described in detail with reference to the accompanying drawings.

Many changes and modifications to the embodiments described herein can be made. The scope of some changes is discussed herein.

Referring to Fig. 2A, a conductive layer for word line (not shown) is deposited on a silicon substrate 111 and a hard mask film (i.e., a nitride film not shown) is deposited on the conductive layer for word line at a thickness of t9 (1500 to 3200 Å).

A word line pattern 114 having a hard mask pattern 113 on a conductive layer pattern 2 for word line is formed by sequentially etching the hard mask film and the conductive layer for word line.

The conductive layer for word line is preferably formed by using doped silicon, polysilicon, tungsten (W), tungsten nitride (WN), tungsten silicide (WSi_x) or titanium silicide ($TiSi_x$).

A word line pattern 114 is formed by a plasma etching process using a chlorine gas such as CCl_4 or Cl_2 as a source to have a high polishing selectivity ratio to a gate oxide film.

An oxide film spacer 115 is formed at the side of the word line pattern 114, by depositing TEOS(tetraethoxysilicate glass) or silane (SiH_4) base oxide according to a low-pressure CVD process(LP CVD), and blanket-etching the surface of the resulting structure.

An interlayer insulating film 117 is formed by depositing an oxide film at a thickness of t10 (5000 to 8000 Å) and planarized. The source of the oxide film includes BPSG(borophosphosilicate glass), PSG(phosphosilicate glass), FSG(fluorosilicate glass), PE-TEOS(plasma enhanced tetraethoxysilicate glass), PE-SiH_4(plasma enhanced-silane), HDP USG(high density plasma undoped silicate glass), HDP PSG(high density plasma phosphosilicate glass) or APL(atomic planarization layer) oxide, preferably BPSG.

Referring to Fig. 2B, the thickness of the interlayer insulating film 117 decreases from t10 to t12 (4500 to 7500 Å) by the planarization process (t10>t12).

An etching process for forming a contact hole 118 for plug by using a landing plug contact mask (not shown) is performed in a predetermined portion of the cell region. Here, since the upper portion of the hard mask pattern 113 is also etched, the thickness of the hard mask pattern decreases from the initial thickness t9 to t11 (1000 to 2500 Å) (t9>t11).

The etching process is performed by a self-aligned contact (SAC) process using C_4F_8, C_2F_6 or C_3F_8 source having a high polishing selectivity ratio to the nitride film, preferably C_4F_8 source.

Referring to Fig. 2C, a silicon layer 119 is deposited on the entire surface of the resulting structure including the contact hole 118 for plug. Here, the silicon layer 119 has step difference of t13 (1000 to 2000 Å) due to step difference between a region where the contact hole is not formed and a region where the interlayer insulating film is removed to form the contact hole.

Preferably, the silicon layer is formed of doped silicon or polysilicon using SiH_4 or Si_2H_6 source.

A plug 121 is isolated by a succeeding polishing process. Preferably, a thickness to be removed is greater than t14 (2200 to 3200 Å).

Referring to Fig. 2D, a CMP process is performed on the entire surface of the silicon layer 119 and the interlayer insulating film 117 by using a slurry including an HXO_n compound until the hard mask pattern 113 is exposed, thereby isolating the plug 121.

Preferably, the CMP process is performed by using a hard pad as a polishing pad under the conditions of a polishing pressure of 2 to 6 psi and a table revolution number of 10 to 700 rpm.

Here, the table revolution number is changed according to an operation type of CMP equipment. For example, a rotary type operation is preferably performed within the range of 10 to 200 rpm, and an orbital type operation is preferably performed within the range of 100 to 700 rpm.

A linear type operation is preferably performed within the range of 100 to 700 fpm (feet per minute).

As a result, the step differences are not generated between the layers after the CMP process. Therefore, the upper portion of the interlayer insulating film is not contaminated, and a hard mask film having a thickness of t15 (500 to 1500 Å) is obtained after the polishing process.

The disclosed methods and improved devices resulting therefrom will be better understood by referring to the following examples, which are not intended to be limiting.

I. Preparation of the Disclosed Slurries

Preparation Example 1

To 95 wt% CMP slurry for oxide film including 20 wt% colloidal SiO_2 as abrasive was added 5 wt% $HClO_4$ and strirred. And the resulting mixture was further stirred for about 30 minutes to be completely mixed and stabilized, to prepare a slurry.

Preparation Example 2

To 90 wt% CMP slurry for oxide film including 15 wt% fumed SiO_2 as abrasive was added 1 wt% $HClO_3$ with stirring, and 9 wt% distilled water was mixed. Then, the mixture was further stirred for about 30 minutes to be completely mixed and stabilized, to prepare a slurry.

Preparation Example 3

To 80 wt% CMP slurry for oxide film including 10 wt% Al_2O_3 as abrasive was added 10 wt% $HBrO_3$ with stirring, and 10 wt% distilled water was mixed. Then, the mixture was further stirred for about 30 minutes to be completely mixed and stabilized, to prepare a slurry.

Preparation Example 4

To 90 wt% CMP slurry for oxide film including 1 wt% CeO_2 as abrasive was added 5 wt% HClO with stirring, and 5 wt% distilled water was mixed. Then, the mixture was further stirred for about 30 minutes to be completely mixed and stabilized, to prepare a slurry.

II. CMP Process by Using Disclosed Slurries

Example 1.

A silicon layer is deposited on the surface of interlayer insulating film including the contact hole for plug. Then, a CMP process is performed to remove the silicon layer on the interlayer insulating film using a common slurry for an oxide film until the interlayer insulating film is exposed.

A CMP process was performed on a silicon layer and an interlayer insulating film under a polishing pressure of 3psi and a table revolution number of 600 rpm, by using the slurry composition of Preparation Example 1, and an orbital operation type polishing equipment until the hard mask pattern is exposed.

Step differences were not generated between the layers and the interlayer insulating film was not contaminated after the CMP process, to form a stable plug.

Example 2.

A silicon layer is deposited on the surface of interlayer insulating film including the contact hole for plug. Then, a CMP process is performed to remove the silicon layer on the interlayer insulating film using a common slurry for an oxide film until the interlayer insulating film is exposed.

A CMP process was performed on a silicon layer and an interlayer insulating film under a polishing pressure of 3 psi and a table revolution number of 600 rpm, by using the

slurry composition of Preparation Example 2, and an orbital operation type polishing equipment until the hard mask pattern is exposed.

Step differences were not generated between the layers and the interlayer insulating film was not contaminated after the CMP process, to form a stable plug.

Example 3.

A silicon layer is deposited on the surface of interlayer insulating film including the contact hole for plug. Then, a CMP process is performed to remove the silicon layer on the interlayer insulating film using a common slurry for an oxide film until the interlayer insulating film is exposed.

A CMP process was performed on a silicon layer and an interlayer insulating film under a polishing pressure of 3 psi and a table revolution number of 600 rpm, by using the slurry composition of Preparation Example 3, and an orbital operation type polishing equipment until the hard mask pattern is exposed.

Step differences were not generated between the layers and the interlayer insulating film was not contaminated after the CMP process, to form a stable plug.

Example 4.

A silicon layer is deposited on the surface of interlayer insulating film including the contact hole for plug. Then, a CMP process is performed to remove the silicon layer on the interlayer insulating film using a common slurry for an oxide film until the interlayer insulating film is exposed.

A CMP process was performed on a silicon layer and an interlayer insulating film under a polishing pressure of 3psi and a table revolution number of 600 rpm, by using the slurry composition of Preparation Example 4, and an orbital operation type polishing equipment until the hard mask pattern is exposed.

Step differences were not generated between the layers and the interlayer insulating film was not contaminated after the CMP process, to form a stable plug.

As discussed earlier, the CMP slurry for oxide film including the HXOn compound, and the CMP process using the same allow the respective multiple layers to have a similar polishing selectivity ratio, to prevent substantial step differences from occurring after the polishing process.

Moreover, polishing residues of each layer and slurry residues are not filled in the upper portion of the interlayer insulating film, a bridge is not generated between a word line and a storage node contact, and leakage current and a mis-alignment of the succeeding process are reduced, which results in a high manufacturing yield.